

1. A device comprising:
 - a silicon chip comprising a plurality of execution units;
 - wherein the plurality of execution units jointly comprise a first plurality of custom silicon arithmetic elements;
 - wherein at least one of the first plurality of custom silicon arithmetic elements is adapted to execute a first multiplication operation
 - on one or more first input signals that represent a first numerical value using a floating point representation that has a signed binary mantissa of no more than 11 bits and a signed binary exponent of at least 6 bits,
 - and on one or more second input signals that represent a second numerical value using a floating point representation;
 - wherein a total number of the first plurality of custom silicon arithmetic elements in the silicon chip that are adapted to execute first multiplication operations exceeds, by at least 1000 more than three times, a total number of second custom silicon arithmetic elements in the silicon chip adapted to perform on each cycle the operation of traditional high-precision multiplication on floating point numbers that are at least 32 bits wide; and
 - wherein the first plurality of custom silicon arithmetic elements are adapted to collectively perform, per cycle, at least tens of thousands of first multiplication operations.
2. The device of claim 1, wherein at least two of the first plurality of custom silicon arithmetic elements share circuitry.
3. The device of claim 1, wherein at least two of the plurality of execution units share circuitry.
4. The device of claim 1, wherein at least one of the plurality of execution units further comprises an arithmetic element implemented using Field Programmable Gate Array (FPGA) reconfigurable logic configured to perform an arithmetic operation.

5. The device of claim 1, wherein each of the plurality of execution units is adapted to execute a second operation on one or more third input signals that represent one or more third numerical values to produce one or more output signals that represent a fourth numerical value; wherein the dynamic range of the third numerical values represented by at least one of the third input signals is at least as wide as from $1/1,000,000$ through $1,000,000$; and wherein for each of at least $X=10\%$ of the possible valid inputs to the second operation the numerical value represented by the one or more output signals differs by at least $Y=.05\%$ from the result of an exact mathematical calculation of the second operation on the numerical values of that input.
6. The device of claim 1, wherein each of the plurality of execution units is adapted to execute a second operation on one or more third input signals that represent one or more third numerical values to produce one or more output signals that represent a fourth numerical value; wherein the dynamic range of the third numerical values represented by at least one of the third input signals is at least as wide as from $1/1,000,000$ through $1,000,000$; and wherein the second operation is nondeterministic and for each of at least $X=10\%$ of the possible valid inputs to the second operation the statistical mean, over repeated execution of the second operation on each specific input from the at least $X\%$ of the possible valid inputs to the second operation, of the numerical values represented by the one or more output signals of the execution unit executing the second operation on that input differs by at least $Y=.05\%$ from the result of an exact mathematical calculation of the second operation on the numerical values of that same input.
7. The device of claim 1, wherein each of the first plurality of custom silicon arithmetic elements is smaller than each of the second plurality of custom silicon arithmetic elements.
8. The device of claim 5, wherein each of the first plurality of custom silicon arithmetic elements is smaller than each of the second plurality of custom silicon arithmetic elements.
9. The device of claim 6, wherein each of the first plurality of custom silicon arithmetic elements is smaller than each of the second plurality of custom silicon arithmetic elements.
10. The device of claim 1, wherein the first multiplication operation is part of forming a weighted sum.

11. The device of claim 5, wherein the first multiplication operation is part of forming a weighted sum.
12. The device of claim 6, wherein the first multiplication operation is part of forming a weighted sum.
13. The device of claim 7, wherein the first multiplication operation is part of forming a weighted sum.
14. The device of claim 8, wherein the first multiplication operation is part of forming a weighted sum.
15. The device of claim 9, wherein the first multiplication operation is part of forming a weighted sum.
16. The device of claim 10, wherein the device further comprises a processor capable of executing software and adapted to control the operation of at least one of the plurality of execution units; and wherein the first multiplication operation is performed as part of the execution by the processor of software programmed to see, hear, or understand.
17. The device of claim 11, wherein the device further comprises a processor capable of executing software and adapted to control the operation of at least one of the plurality of execution units; and wherein the first multiplication operation is performed as part of the execution by the processor of software programmed to see, hear, or understand.
18. The device of claim 12, wherein the device further comprises a processor capable of executing software and adapted to control the operation of at least one of the plurality of execution units; and wherein the first multiplication operation is performed as part of the execution by the processor of software programmed to see, hear, or understand.
19. The device of claim 13, wherein the device further comprises a processor capable of executing software and adapted to control the operation of at least one of the plurality of execution units; and wherein the first multiplication operation is performed as part of the execution by the processor of software programmed to see, hear, or understand.
20. The device of claim 14, wherein the device further comprises a processor capable of executing software and adapted to control the operation of at least one of the plurality of

execution units; and wherein the first multiplication operation is performed as part of the execution by the processor of software programmed to see, hear, or understand.

21. The device of claim 15, wherein the device further comprises a processor capable of executing software and adapted to control the operation of at least one of the plurality of execution units; and wherein the first multiplication operation is performed as part of the execution by the processor of software programmed to see, hear, or understand.

22. The device of claim 1, wherein the first multiplication operation is part of convolving a kernel.

23. The device of claim 5, wherein the first multiplication operation is part of convolving a kernel.

24. The device of claim 6, wherein the first multiplication operation is part of convolving a kernel.

25. The device of claim 7, wherein the first multiplication operation is part of convolving a kernel.

26. The device of claim 8, wherein the first multiplication operation is part of convolving a kernel.

27. The device of claim 9, wherein the first multiplication operation is part of convolving a kernel.

28. The device of claim 1, wherein the device further comprises a processor capable of executing software and adapted to control the operation of at least one of the plurality of execution units; and wherein the first multiplication operation is performed as part of the execution by the processor of software programmed to see, hear, or understand.

29. The device of claim 5, wherein the device further comprises a processor capable of executing software and adapted to control the operation of at least one of the plurality of execution units; and wherein the first multiplication operation is performed as part of the execution by the processor of software programmed to see, hear, or understand.

30. The device of claim 6, wherein the device further comprises a processor capable of executing software and adapted to control the operation of at least one of the plurality of

execution units; and wherein the first multiplication operation is performed as part of the execution by the processor of software programmed to see, hear, or understand.