Singular Computing LLC - United States Patent Application 17/029,780 Claims

1. A method, for use with a silicon chip that has a clock, the method comprising:

completing, in a single cycle of the clock, using the silicon chip, at least tens of thousands of first multiplication operations;

wherein each of the first multiplication operations operates on

a respective first numerical input value represented using a first floating point representation that has a signed binary mantissa of no more than 11 bits and a signed binary exponent of at least 6 bits,

and a respective second numerical input value represented using a second floating point representation; and

wherein the number of the first multiplication operations is at least 1000 more than three times the maximum number of traditional high-precision multiplication operations on floating point numbers at least 32 bits wide that the silicon chip is adapted to complete in a single cycle of the clock.

2. The method of claim 1, further comprising:

before completing the first multiplication operations, completing one or more second arithmetic operations, wherein each of the second arithmetic operations converts a respective third numerical input value represented using a traditional high-precision floating point representation at least 32 bits wide to a respective numerical output value represented using the first floating point representation, thereby generating one or more numerical output values; and

completing the first multiplication operations using one or more of the numerical output values as first numerical input values to one or more of the first multiplication operations.

3. The method of claim 2, wherein each of the second arithmetic operations is deterministic.

4. The method of claim 2, wherein each of the second arithmetic operations is non-deterministic.

5. The method of claim 3, wherein for each of at least X=10% of the possible third numerical input values to the at least one of the second arithmetic operations, the numerical output value differs by at least Y=.05% from the third numerical input value.

6. The method of claim 4, wherein for each of at least X=10% of the possible third numerical input values to the at least one of the second arithmetic operations, the statistical mean of the numerical output values, produced by repeated execution of the at least one of the second arithmetic operations on the third numerical input value, differs by at least Y=.05% from the third numerical input value.

7. The method of claim 1, wherein the silicon chip is a graphics processing unit (GPU).

8. The method of claim 2, wherein the silicon chip is a graphics processing unit (GPU).

9. The method of claim 5, wherein the silicon chip is a graphics processing unit (GPU).

10. The method of claim 6, wherein the silicon chip is a graphics processing unit (GPU).

11. The method of claim 1, wherein the silicon chip is a Field Programmable Gate Array (FPGA).

12. The method of claim 2, wherein the silicon chip is a Field Programmable Gate Array (FPGA).

13. The method of claim 1, wherein the silicon chip is an Application Specific Integrated Circuit (ASIC).

14. The method of claim 2, wherein the silicon chip is an Application Specific Integrated Circuit (ASIC).

15. The method of claim 1, further comprising forming a weighted sum, wherein forming the weighted sum comprises completing at least one of the first multiplication operations.

16. The method of claim 2, further comprising forming a weighted sum, wherein forming the weighted sum comprises completing at least one of the first multiplication operations.

17. The method of claim 7, further comprising forming a weighted sum, wherein forming the weighted sum comprises completing at least one of the first multiplication operations.

18. The method of claim 8, further comprising forming a weighted sum, wherein forming the weighted sum comprises completing at least one of the first multiplication operations.

19. The method of claim 9, further comprising forming a weighted sum, wherein forming the weighted sum comprises completing at least one of the first multiplication operations.

20. The method of claim 10, further comprising forming a weighted sum, wherein forming the weighted sum comprises completing at least one of the first multiplication operations.

21. The method of claim 11, further comprising forming a weighted sum, wherein forming the weighted sum comprises completing at least one of the first multiplication operations.

22. The method of claim 12, further comprising forming a weighted sum, wherein forming the weighted sum comprises completing at least one of the first multiplication operations.

23. The method of claim 13, further comprising forming a weighted sum, wherein forming the weighted sum comprises completing at least one of the first multiplication operations.

24. The method of claim 14, further comprising forming a weighted sum, wherein forming the weighted sum comprises completing at least one of the first multiplication operations.

25. The method of claim 15, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

26. The method of claim 16, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

27. The method of claim 17, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

28. The method of claim 18, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

29. The method of claim 19, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

30. The method of claim 20, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

31. The method of claim 21, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

32. The method of claim 22, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

33. The method of claim 23, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

34. The method of claim 24, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

35. The method of claim 15, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to process visual information.

36. The method of claim 16, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to process visual information.

37. The method of claim 1, further comprising convolving a kernel, wherein convolving the kernel comprises completing at least one of the first multiplication operations.

38. The method of claim 2, further comprising convolving a kernel, wherein convolving the kernel comprises completing at least one of the first multiplication operations.

39. The method of claim 7, further comprising convolving a kernel, wherein convolving the kernel comprises completing at least one of the first multiplication operations.

40. The method of claim 8, further comprising convolving a kernel, wherein convolving the kernel comprises completing at least one of the first multiplication operations.

41. The method of claim 9, further comprising convolving a kernel, wherein convolving the kernel comprises completing at least one of the first multiplication operations.

42. The method of claim 10, further comprising convolving a kernel, wherein convolving the kernel comprises completing at least one of the first multiplication operations.

43. The method of claim 11, further comprising convolving a kernel, wherein convolving the kernel comprises completing at least one of the first multiplication operations.

44. The method of claim 12, further comprising convolving a kernel, wherein convolving the kernel comprises completing at least one of the first multiplication operations.

45. The method of claim 13, further comprising convolving a kernel, wherein convolving the kernel comprises completing at least one of the first multiplication operations.

46. The method of claim 14, further comprising convolving a kernel, wherein convolving the kernel comprises completing at least one of the first multiplication operations.

47. The method of claim 37, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

48. The method of claim 38, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

49. The method of claim 39, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

50. The method of claim 40, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

51. The method of claim 41, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

52. The method of claim 42, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

53. The method of claim 43, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

54. The method of claim 44, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

55. The method of claim 45, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

56. The method of claim 46, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to see, hear, or understand.

57. The method of claim 37, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to process visual information.

58. The method of claim 38, wherein the at least one of the first multiplication operations is performed as part of the execution by the silicon chip of software programmed to process visual information.

59. The method of claim 1, wherein the first floating point representation is the same as the second floating point representation.